FINAL PROGRESS REPORT
PHASE I

MONOLITHIC PARALLEL PROCESSOR

(28 DECEMBER 1968 TO 27 JANUARY 1970)

CONTRACT NO. NAS 5-11577

Prepared by

RCA ELECTRONIC COMPONENTS
Somerville, New Jersey

for

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

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GODDARD SPACE FLIGHT CENTER
CONTRACTING OFFICER: A.L. ESSEX
TECHNICAL MONITOR: F. LINK

PREPARED BY

RCA ELECTRONIC COMPONENTS
Somerville, New Jersey

PROJECT MANAGER: H. WEISBERG
PROJECT ENGINEER: A. DINGWALL

for

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

ABSTRACT

A four-bit parallel processor LSI array was designed and fabricated using COS/MOS integrated-circuit technology. Functional packaged units were delivered to NASA to demonstrate achievement of Phase I goals and to show the applicability of techniques for high-yield processing. The design features include the provision for interconnecting groups of parallel processor chips to form an expanded processor of any desired word length. This 800-transistor "computer on a chip" circuit has the logic capability of a medium-size, medium-speed, general-purpose computer suitable for sophisticated scientific data processing. The demonstration of functional circuits represented a significant milestone in IC technology.

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SECTION I
INTRODUCTION

An 18-month developmental program was conducted to design, develop, and fabricate monolithic complementary-symmetry MOS (COS/MOS) large-scale parallel processor arrays. This task was completed successfully, on a developmental basis, and parallel processor arrays of 800-transistor complexity were designed, fabricated, and tested and were delivered to the NASA Goddard Space Flight Center.

The successful achievement of Phase I goals for the parallel processor was the result of the coordinated efforts of the NASA Goddard Space Flight Center and RCA. The original concept of functional operation of the array were conceived by R. J. Lesniewski [1-3] of the NASA Goddard Space Flight Center as part of a program to realize an ultralow-power computer that requires a minimal number of array types. The logic was extended and techniques for interconnecting groups of chips were implemented by RCA Airborne Systems Division, Burlington, Massachusetts, and by RCA Electronic Components, Somerville, New Jersey.

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1 Lesniewski, R. J., "A Large Scale Integration (LSI) Computer Concept Utilizing only Five Types of General Purpose Digital Arrays," Master of Science Thesis, University of Maryland; 1970.

2 Lesniewski, R. J., and Link, F. J., "A Complementary - MOS Space Craft Data Handling System," Proc. GOMAC Conference, 1969.

3 Lesniewski, R. J., and Schaefer, D. H., "Goddard Space Flight Center Ultra Low Power Computer Development Program," Proc. Third NASA Intracenter Microelectronics Conference, February 1968.

SECTION II
PARALLEL PROCESSOR DESIGN

A. GENERAL

The COS/MOS four-bit parallel processor IC is a "computer on a single chip" device with an equivalent logic complexity of 200 input gates. The parallel processor has the capability of a small-size, medium-speed, general-purpose computer (except for memory and data buffering).

A unique feature of the parallel processor is the provision for interconnecting several units to form a computer with the capability of the desired word length. The capability of 16-bit word length, for example, can be achieved with four units; the resulting configuration would be typical of the computer size that would be suitable for sophisticated on-line scientific data processing.

The 16-instruction repertoire of the parallel processor enables a circuit capability for performing many complex functions, which include:

a. Addition
b. Subtraction
c. Multiplication
d. Division
e. AND
f. OR
g. EXCLUSIVE-OR
h. Data Storage
i. Sign Detection
j. Double Precision Arithmetic

The power-dissipation goals of the COS/MOS parallel processor were particularly low: 100 microwatts during standby; 10 milliwatts during the time of calculation at a 500-kilohertz clock rate.

The device was fabricated successfully on a large chip (146 mils by 155 mils). Achieving large-chip fabrication using high-yield processing techniques of a device with this high level of logic complexity is a milestone in COS/MOS IC technology.

B. LOGIC DESIGN

Details of the four-bit parallel processor array design and function were discussed in the first interim report.[3] This report may be consulted for detailed information relating to functions, operational codes, pin connections, and interconnections for expanding four-bit arrays to provide 16-bit (or larger) processors.

Figure 1 is a photograph of the array chip. The overall logic diagram of the parallel processor is shown in Figure 2.

Item	Description
Chip size (mils)	146 by 155
Number of devices	800
Number of pads	27 (four for expansion)
Package	28-lead flatpack

1. ARRAY FUNCTIONAL CAPABILITIES

The block diagram of Figure 3 illustrates the organization of the array. The functional- and mode-control section accepts four functional-control signals, to provide the 16 basic array operations, and two mode-control signals. Mode control governs the operation of the overflow structure and modifies the carry and serial-shift input and output such that the array can be used as any four-bit section of a larger arithmetic unit. The shift/store register, which contains four storage registers, performs the following functions: shift-left and shift-right operations; and parallel input and output of data to and from the parallel data lines or the arithmetic processor section. The arithmetic processor section can perform four-bit parallel 1's- or 2's-complement additions and subtractions, counting, and logic functions. During arithmetic operations, a fast-carry structure is used to minimize the carry-propagate time. The array also can detect, correct for, and indicate arithmetic overflow conditions. In addition to the functions just described, the array has inputs and outputs for performing the functions of zero indication, negative indication, and conditional control. Conditional

[3] Monolithic Parallel Processor, Periodic Progress Report, Contract NAS 5-11577 (December 1968)

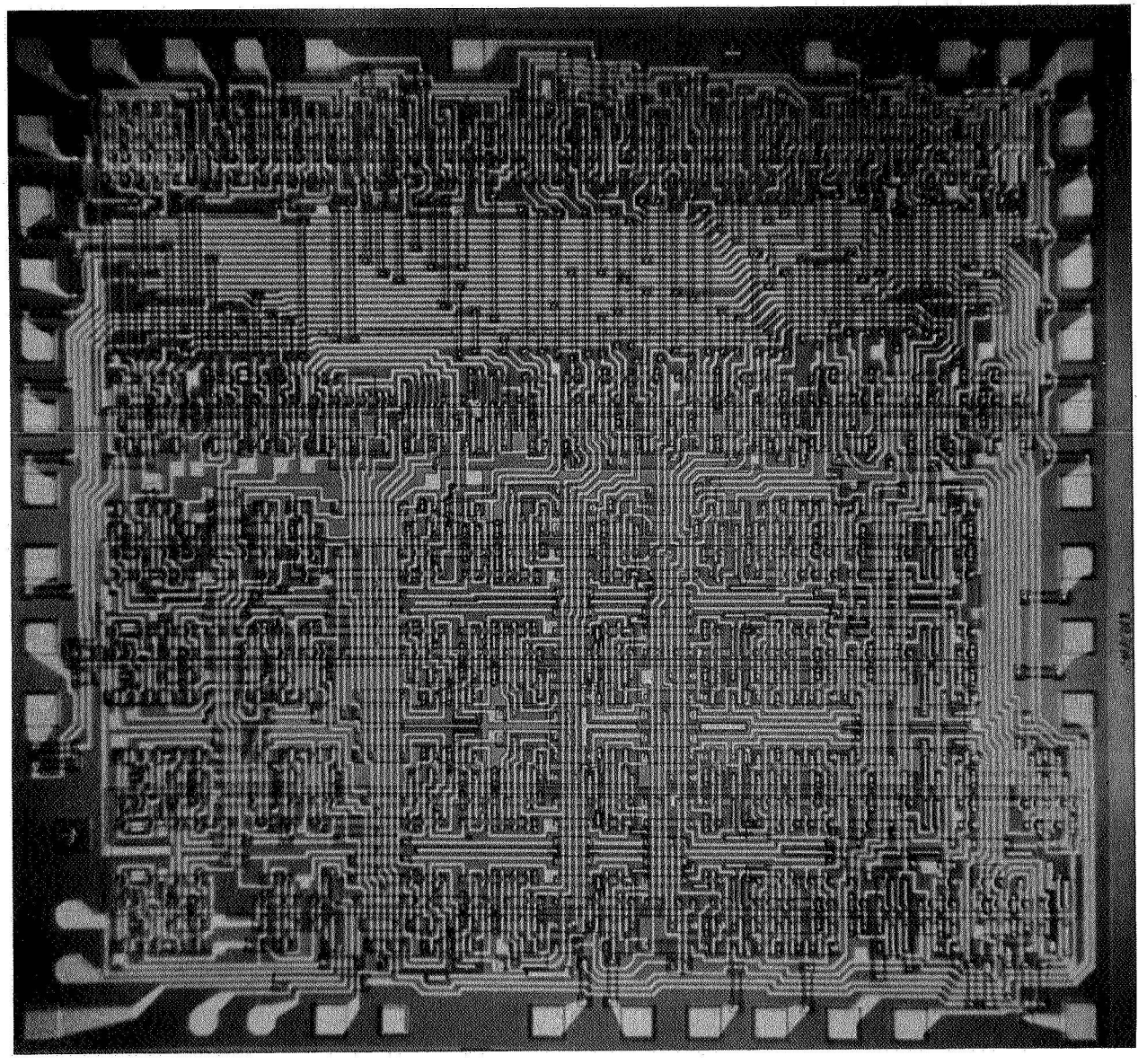

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Figure 1. Parallel Processor, Array Chip

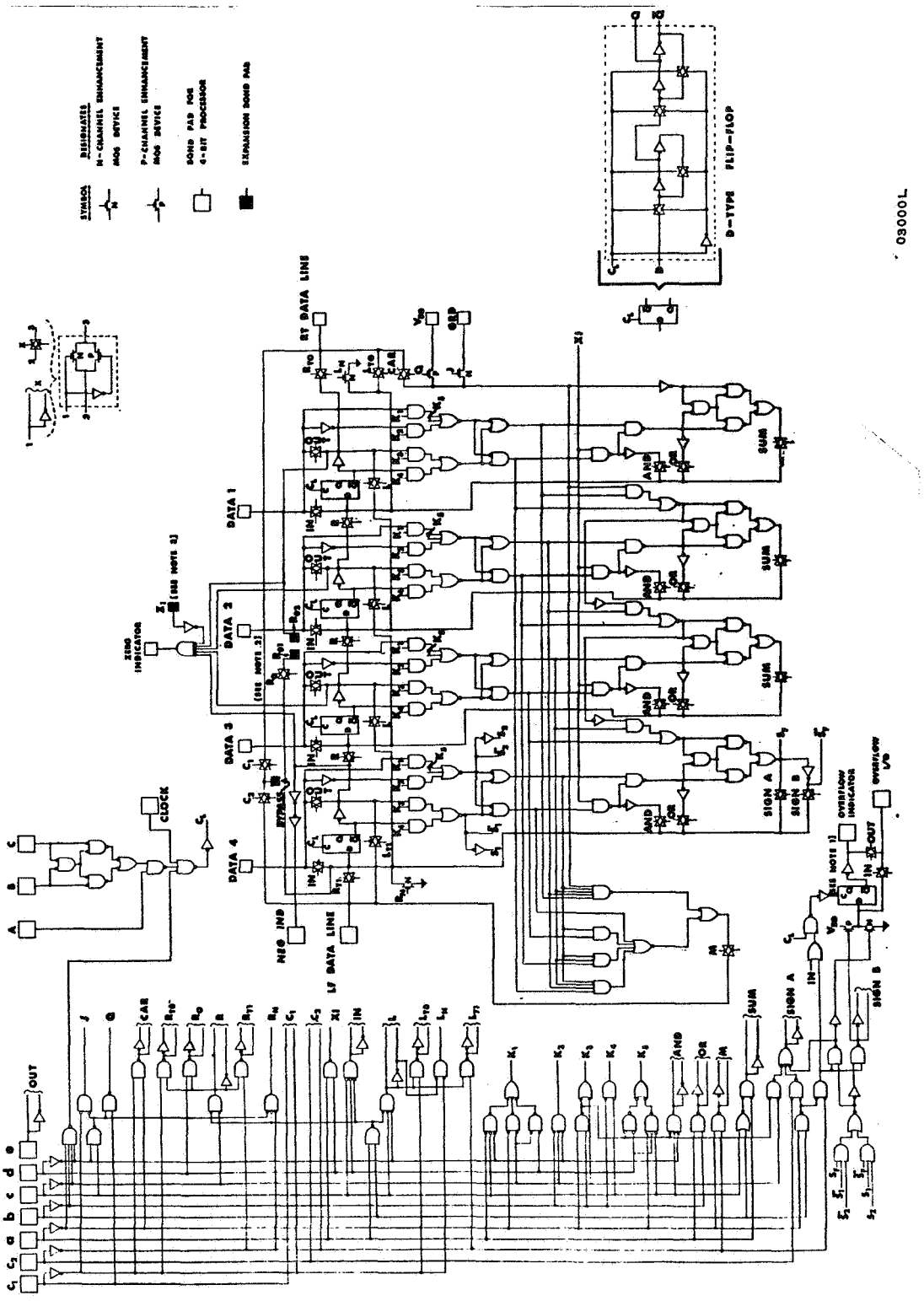

Figure 2. Logic Diagram

NOTE 1. D-TYPE FLIP-FLOP TRANSFERS D INPUT TO Q OUTPUT ON LOW-GO-HIGH CLOCK TRANSITION.

NOTE 2. R_{01} CONNECTED TO A_{03} FOR 4-BIT PROCESSOR.

NOTE 3. IF Z_1 IS UNUSED, CONNECT IT TO V_{DD}.

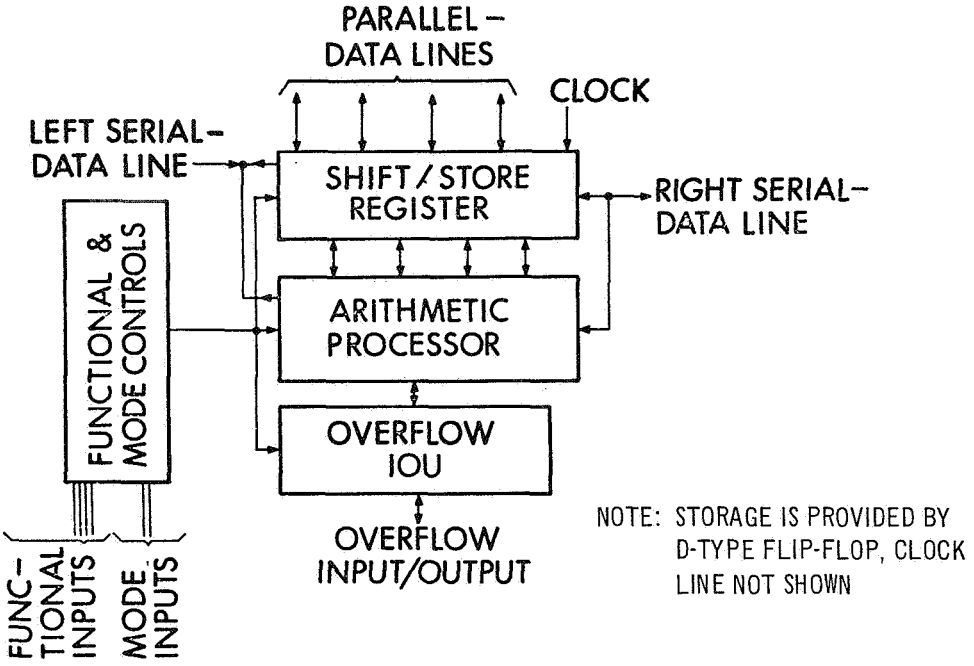

Figure 3. One Bit of Shift/Store and Arithmetic Processor Logic

control inhibits array processing during interrupts. The functional repertoire of the basic array is summarized in Table I.

2. LOGIC IMPLEMENTATION

To implement effectively a random-logic array of this functional complexity, transmission-gate data routing and functional gating were used, where feasible, to obtain substantial reduction of the device requirements. Figure 4 shows the logic for one bit of the data-handling portion of the array to illustrate the use of transmission gates for controlling logic paths and to provide insight into the data flow required of the array.

Transmission gating reduces the logic required by controlling the data paths. As shown in Figure 4, data from one of six possible sources is made available for strobing into the flip-flop. If an ADD function is being executed, for example, the "sum" transmission gate is activated by the functional-control logic, while the other five transmission gates are inactivated. The output of the EXCLUSIVE-OR gate, therefore, is made available at the flip-flop data input, where it can be clocked into storage. Using edge-sensitive D-type flip-flops eliminates concern over recirculating data.

Functional gating synthesizes the Boolean logic expression directly with components in a single-stage, relay-type operation. Figure 5 shows an example of functional gating in which the logic expression represents a partial carry of the output fast-carry structure. To implement this expression using standard NAND/NOR gating, 26 devices (one p-type device and one n-type device for each gate input) would be required; however, the functional realization requires only 14 devices.

Functional gating is extremely attractive in COS/MOS technology due to the fact that only p-type and n-type active devices are required. A pair of p- and n-type devices constitutes a basic decision-making element with a single common input to the gate of each device; the devices always operate as a pair, with one device on and the other off. There is no load current; the output is either at supply voltage or at ground potential; there is no

TABLE I

ARRAY FUNCTIONS

NO-OP (operational inhibit)
Left shift
Right shift
Rotate cycle (shift)
Input data (from parallel-data lines)
Clear to zero
Set to one
Count up
Count down
Add
Subtract (memory from stored number)
Subtract (stored number from memory)
Subtract from zero (stored number)
AND
OR
EXCLUSIVE-OR

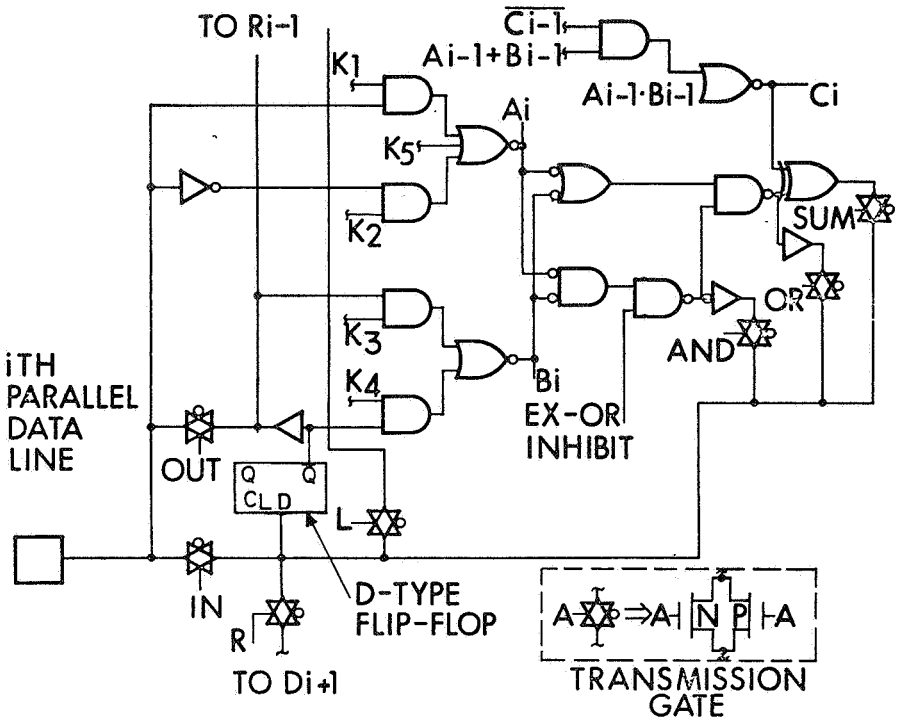

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Figure 4. Logic for Fast-Carry Output

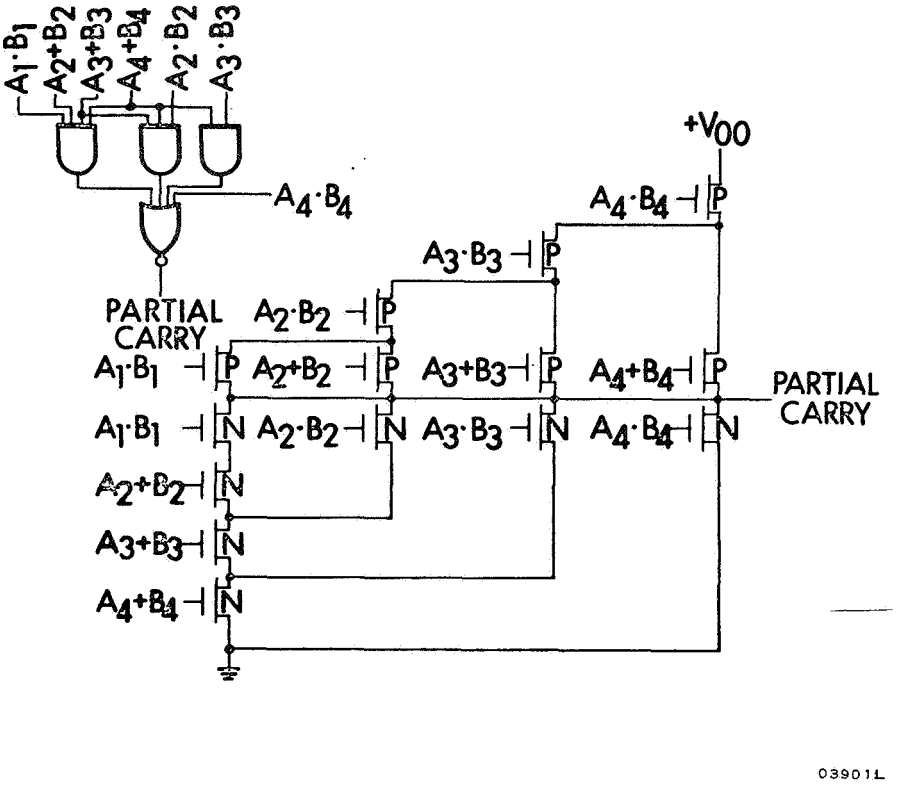

Figure 5. Boolean Expression of Functional Grating for Fast-Carry Output

level shifting (because inputs and outputs are at the same potential); and they may be combined in series or parallel configurations with other p- and n-type pairs without restriction.

In the functional synthesis of a Boolean equation, the n-type devices are configured to synthesize an "active high input" logic structure in a relay-type logic form, as in Figure 5. This configuration of devices will supply a path from the output to ground for the active logic states. For all inactive states, a path must be supplied to the positive potential. This path is accomplished by configuring the p-type devices in a relay logic form that realizes the complement of the desired Boolean expression. For an "input active low" logic structure, p-type devices synthesize the Boolean equation in relay-logic form from the output to plus V, and the n-type devices provide the path to ground for the inactive states. If only NAND/NOR gating is used to implement this array, more than 20 percent additional devices would be required.

Figure 4 illustrates the timing involved in executing an instruction. In a typical data-processing role, the array will accept a word on the parallel-data lines and will clock the word into the flip-flops while applying the "in" control instruction. The second word then will be applied to the data lines, and the desired control will be decoded to activate appropriate gate controls and transmission gates, providing a result at the flip-flop inputs. This data then is clocked into the flip-flops prior to applying the "out" command.

C. ELECTRICAL PERFORMANCE

In spite of the limited number of samples of parallel processor units tested and the complexity of the circuit, it was possible to characterize the general electrical performance of the parallel processor. Based upon both computer computations and limited electrical measurements, the worst-case four-bit addition is approximately 1.5 microseconds at V_{DD} = 10 volts. The design objective for a data-transfer rate of 2.0 microseconds, therefore, was attained. Because speed depends somewhat upon processing and operating

power, additional data would be required to determine whether all functional parallel processors met a 2.0-microsecond limit.

An important feature of COS-MOS circuits is that standby power dissipation is due only to DC leakage levels, which can be as low as 10^{-12} ampere per transistor. Imperfect registration of the photomasks used to fabricate the parallel processor (see Paragraph III.B), however, reduced normal dimensional clearances. The resulting close proximity of reverse-biased n^+ and p^+ diffusions reduced maximum operating voltage ratings and contributed to increased leakage levels. Standby power dissipation of the 800-transistor parallel processor samples fabricated during this Phase I study typically was 1 to 2 milliwatts. This level, although low compared to those obtained using other IC technologies for a 800-transistor device, can be improved significantly by using improved photomasks that meet the tolerances for commercial COS/MOS devices.

SECTION III
FABRICATION AND TESTING

A. GENERAL

Successful fabrication of parallel processors represents a definite advance in COS/MOS technology. In retrospect, design and fabrication of the parallel processor for Phase I entailed considerably more effort in most areas than originally was anticipated. Technical problem areas in photomasking were uncovered that had not been foreseen at the start of the program.

The design of the parallel processor is more complex than that required for commercial COS/MOS devices, with respect to large device count (800 transistors), large chip size (146 mils by 155 mils), and generally "random" logic. In respect to device count alone, this represents a five-fold increase in complexity over the most complex devices available at the start of the program. General "randomness" of the logic, as compared to the "regular" logic of present commercial counters, registers, and memory cells, was manifested in difficult and space-consuming layouts, due to large numbers of interconnections running the entire length of the chip; nonrepetitive local layouts requiring extensive design effort; and other than simple testing and debugging procedures. Because IC yield decreases exponentially with device count, high-yield techniques were required to ensure reasonable yields. Despite such technical challenges, parallel processor units were designed and fabricated successfully, and the feasibility of COS/MOS chips with this level of logical complexity was demonstrated.

B. FABRICATION

During the course of the Phase I study, it became apparent that the major, and generally unanticipated, technical difficulty would be to obtain large-chip-size, low-defect-level photomasks of good resolution and dimensional fidelity. The photomasks used to make parallel processor units could be

rejected on several counts by commercial COS/MOS device standards. These limitations are associated with prior state-of-the-art piecing techniques of photomask fabrication for large chips, using hand-cut Rubylith artwork (at 500X scale) and multiple photographic reductions. Recent advances in the state of the art, based upon computer-generated reticles, however, would have eliminated these difficulties, and RCA would recommend this approach in any further development.

Because the large chip size (155 mils by 146 mils) of the parallel processor exceeded the maximum useful capability of the reducing lenses, each photomask had to be prepared in four parts, and each quadrant had to be step-and-repeated individually. In this process, it was necessary to insert each reticle "blind" into the photorepeater. It was observed that the accuracy with which each quadrant could be located mechanically, with respect to its neighbors, was such that the desired maximum design tolerance of 50 microinches could not be maintained consistently, and random positioning errors greater than 100 microinches resulted within a chip.

The pattern misregistration just described cannot be tolerated in the COS/MOS fabrication-sequence procedure, which requires successive alignments of seven photomasks, each subject to independent, random, quadrant location. In three masks (n^+, p^+, and metalization), relative alignment is absolutely critical to avoid shorts and/or to ensure that the gate metal overlaps both source and drain diffusions for proper MOS transistor operation.

Extraordinary alignment techniques were needed for the limited number of parallel processors that were fabricated under the Phase I program. After studying random make runouts, engineering personnel familiar with the circuit topology were required for the deliberate and precise "misalignment" of each mask to obtain the best "compromise misalignment" and/or to compose photoresist images by using multiple exposures and/or vignetting "tricks" in critical alignment stages. Such techniques are not adequate to support a reproducible or high-yield process for more than a limited supply of parallel processor engineering samples. Conventional design clearances between n^+ and p^+ diffusions and gate metal overlap could not be maintained consistently;

consequently, many wafers fabricated were "shorted" or totally dead because the optimum degree of misregistry could not be obtained.

To fabricate additional large-chip COS/MOS devices routinely and successfully, better mask-fabrication methods were required. At this point in time, RCA would employ new and technically superior photomask equipment; however, this equipment was not available to the industry at the start of the program. The superior approach would entail using computer-prepared 10X reticles from digitized design information and an ultramodern photorepeater.

C. TESTING PARALLEL PROCESSOR LOGIC

Because of the complexity of parallel processor logic, major effort was devoted to ensuring that the parallel processor chip layout reflected accurately the logic shown in Figure 2. Five basic checks were employed:

a. Six independent checks of artwork by RCA and NASA engineers.

b. Random electrical checks of the chip repertoire at RCA.

c. Electrical microprobing of parallel processor chips to verify truth tables locally.

d. Electrical test sequence of 320 tests, performed with a computer test set.

e. Preliminary checks of delivered units at NASA Goddard.

The results of each basic check indicated that the parallel processor design implemented correctly the desired logic shown in Figure 1.

A reasonably detailed logic check of parallel processor layouts requires approximately five working days. Six such checks were conducted independently by engineers from RCA and NASA. Subsequent electrical testing indicated that only one significant layout error was overlooked in this test procedure (a lower-case "c" control line being tied erroneously to an adjacent upper-case "C" line). Two additional errors were introduced during the mask-making process, due to faulty piecing. These errors were detected by subsequent electrical testing.

The two basic methods for testing parallel processor units electrically also provided independent checks of the correctness of the logic. Electrical microprobing first was performed under a 50X microscope, using micrometer-manipulated needles with 1/4-mil-radius tips, to sense the signals on each aluminum interconnect. By applying a series of 16 time-sequenced pulses to the external input controls and, if required, to internal nodes, local electrical truth tables for the entire 16-instruction repertoire at every connection could be verified by comparing observed responses with calculated responses. In this manner, the entire circuit was checked logically in a 10-week study. The second basic approach was a final test program of 320 tests, which were designed to exercise each gate of the parallel processor from external inputs. The delivered parallel processor units passed this 320-test sequence successfully.

SECTION IV
CONCLUSIONS AND RECOMMENDATIONS

A four-bit parallel processor was designed and fabricated during the Phase I study. The logic design conformed to the contract objectives. The array of 800 devices requires a silicon chip 146 mils by 155 mils. Functional samples were delivered to the NASA Goddard Space Flight Center for evaluation and the feasibility of the approach was demonstrated.

The major technical problem encountered was that the set of photomasks, which was prepared with best 1969 state-of-the-art Rubylith and photographic-reduction techniques, did not register with sufficient accuracy to permit repeatable fabrication of samples. RCA recommends digitizing of the now-debugged design data to make superior-quality, computer-generated photomask reticles.

SECTION V

NEW TECHNOLOGY

After a diligent review of the work performed under this contract, it was determined that no new innovation, discovery, improvement, or invention was made.